owner's manual

BG-BANK 256S

256 kilobyte Static Memory

BG COMPUTER APPLICATIONS

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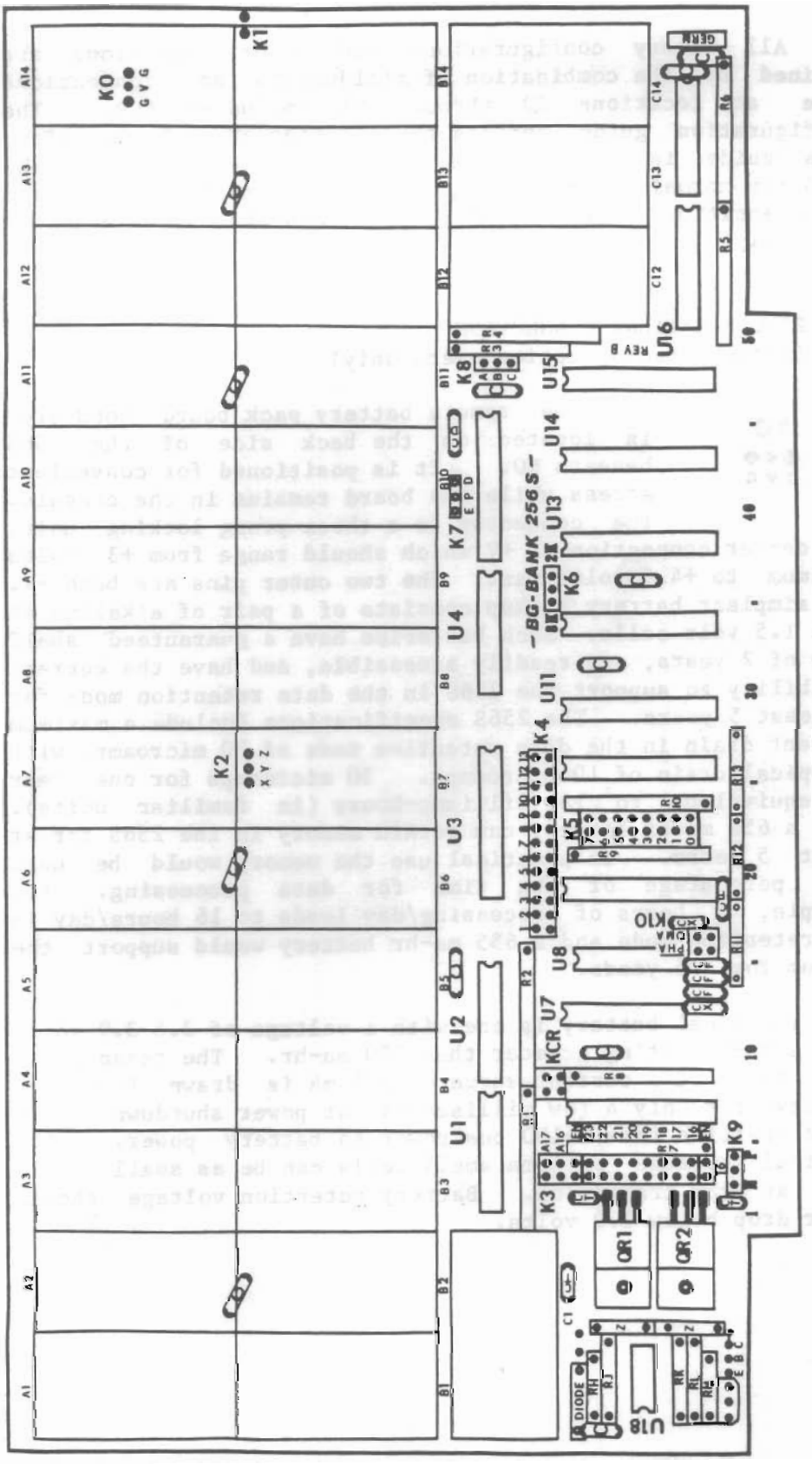
BG-BANK 256S

REFERENCE MANUAL

revision 2.0

TABLE OF CONTENTS

I. BG-BANK 256S IC and JUMPER AREA PATTERN



II. BG-BANK 256S CONFIGURATION GUIDE

All memory configurations and memory functions are defined by the combination of minijumpers and connections made at locations K0 through K10 including KCR. The configuration guide defines the function of each location. This guide is intended to help a user quickly arrange the 256S for normal memory arrangements. For more sophisticated implementation, the technical sections should be examined carefully.

K0: REMOTE BATTERY CONNECTION
(Battery backup option users only)

The remote battery pack board connector is located on the back side of the 256S beneath K0. It is positioned for convenient access while the board remains in the chassis. The connector is a three prong locking unit. The center connection is +V which should range from +3 volts minimum to +4.5 volts max. The two outer pins are both -V. The simplest battery backup consists of a pair of alkaline AA size 1.5 volt cells. Such batteries have a guaranteed shelf life of 2 years, are readily accessible, and have the current capability to support the 256S in the data retention mode for at least 5 years. The 256S specifications include a maximum current drain in the data retention mode of 30 microamps with a typical drain of 10 microamps. 30 microamps for one year is equivalent to 131 milliamp-hours (in familiar units). Thus a 655 ma-hr battery can retain memory in the 256S for at least 5 years. In practical use the memory would be used some percentage of the time for data processing. For example, 8 hours of processing/day leads to 16 hours/day in the retention mode and a 655 ma-hr battery would support the system for 7.5 years.

The ideal battery is one with a voltage of 3.6-3.9 volts and a ma-hr rating greater then 300 ma-hr. The reason for this is that a current surge of 3-5 mA is drawn from the battery for only a few milliseconds at power shutdown during the transition from S-100 bus power to battery power. The terminal voltage of some small cells can be as small as 1 volt at the transition. Battery retention voltage should never drop below 2.0 volts.

K1-K2: POWER DISTRIBUTION FOR RAM-EPROM MIXING
(Battery backup option users only)

The two areas labeled K1 and K2 on the 256S IC and jumper area pattern layout (page 1) are points where the power distribution bus to the memory can be cut to isolate a block of 8 memory chip locations. The memory block is B7-B14. This isolation allows mixing of EPROM and battery-backed ram. If battery backup is not used, EPROM may be mixed with RAM. However, if the battery backup option is used, the EPROM would quickly drain the battery power at shutdown. Isolating the bus allows the 8 chip block to be powered by the normal +5 volt TTL supply voltage while the remaining 24 memory locations are powered by the dual power bus (+5 and Battery). The bus isolation is done on the back side of the board at the points K1 and K2. However, there are no labels on the back side. The prodedure is:

1. Cut PC trace at K1 to disconnect edge vertical trace from the horizontal memory bus trace.
2. Cut the PC trace at K2 severing the trace line that connects X and Z.
3. Solder a small jumper wire between Y and Z.

The memory block B7-B14 is now powered by the +5 volt TTL power supply. The remaining memory is supported by the battery if a battery pack is connected and the S-100 bus power is turned off.

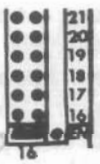
K3: 3,4-11: EXTENDED ADDRESSING

If extended addressing is to be used, a shorting jumper is placed at K3 position 3. If the memory is to be in a 256K window, jumpers are also placed at K3 positions 1 and 2 and jumpers must be left off of K3 positions 10 and 11. Positions 4 through 11 correspond to extended addresses A23 through A16. The 256K window is chosen by selecting A18 through A23. No jumper corresponds to an address of 0.

If extended addressing is to be used and the memory is used as a 128K block, jumpers must be at K3 positions 2 and 3 and not at position 11. Jumpers at K3 positions 4 through 10 select the 128K window by configuring addresses A23 through A17.

If extended addressing is used and the memory is to be in a 64K window, a jumper at K3 position 3 is required. The 64K window is selected by jumpers at K3 positions 4 through 11 configuring addresses A23 through A16.

K3-12: 8/16 BIT DATA TRANSFERS



If the board is to accommodate 16 bit data transfers, a jumper should be installed at K3 position 12. This inputs the 16-REQUEST line of the S-100 bus to the STATUS prom to correctly define the data paths. No jumper at K3-12 means 8-bit transfers only.

KCR: CROMIX-D COMPATIBILITY

The jumper area KCR is only used with CROMEMCO systems operating under CROMIX-D. If the board is used under CROMIX-D, two vertical jumpers must be installed at KCR and the special CROMEMCO PROM set must be implemented (see memory configurations).

K4: 256S MEMORY CONFIGURATIONS

All memory banking arrangements are determined by PROMS. The configuration used is determined by the jumper arrangement at K4 and for some arrangements the extended address arrangement at K3.

A. 256K LINEAR MEMORY:

The memory is addressed as 256K of continuous memory. The memory may be in any 256K window defined by jumpers at A18-A23 of the extended address jumper, K3:4-9.

BANK SELECT CONTROLS: The memory is not banked in the linear 256K configuration. However, I/O controls may be output to WRITE-PROTECT blocks of memory from the top 64K to the total memory. The following table assumes that the 256K of memory is located in the bottom 256K window. The jumper setting at K7 also provides two WRITE-PROTECT options at RESET.

RESET I -NONE-

RESET II -ALL-

Hex output	Write-protected
80	-NONE-
40	30000-3FFFF (top 64K)
20	28000-3FFFF (top 96K)
10	20000-3FFFF (top 128K)
08	18000-3FFFF (top 160K)
04	10000-3FFFF (top 192K)
02	08000-3FFFF (top 224K)
01	00000-3FFFF (-ALL-)
00	-NONE-

Any other output through the I/O port removes all WRITE-PROTECT.

B: LINEAR MEMORY-64K (256S populated with 2Kx8 ram chips)

The memory is addressed as 64K of continuous memory. The memory may be in any 64K window defined by jumpers A16-A23 of the extended address jumper, K3.

BANK SELECT CONTROLS: The memory is not banked in the linear 64K configuration. However, I/O controls may be output to WRITE-PROTECT blocks of memory from the top 16K to the total memory. The following table assumes that the 64K of memory is located in the lowest 64K window. The jumper setting at K7 also provides two WRITE-PROTECT options at RESET.

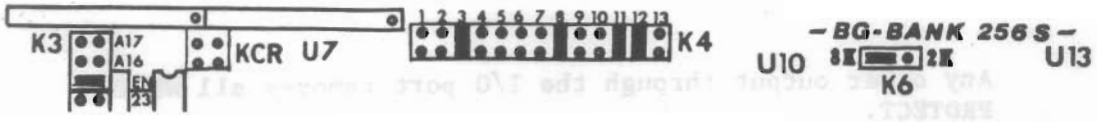
RESET I -NONE-

RESET II -ALL-

Hex output	Write protected
80	-NONE-
40	C000-FFFF (top 16K)
20	A000-FFFF (top 24K)
10	8000-FFFF (top 32K)
08	6000-FFFF (top 40K)
04	4000-FFFF (top 48K)
02	2000-FFFF (top 56K)
01	-ALL MEMORY-
00	-NONE-

Any other output through the I/O Port removes all WRITE-PROTECT.

C. LINEAR-64K of 8Kx8 RAM (partial population)



The memory is addressed as 64K of continuous memory. The memory may be in any 64K window defined by jumpers A16-A23 of the extended address jumper, K3. The 8 memory chips must be installed in the sockets that

correspond to the lowest 64K block of the 256K memory. Those memory locations are A1,A2,A3,A4,A6,A7,A8,and A9. (note: A5 is not part of this block).

BANK SELECT CONTROLS: The memory is not banked in the linear configuration. I/O controls may be output to WRITE-PROTECT the memory. The table assumes that the 64K of memory is located at the bottom of memory. The jumper setting at K7 also provides two WRITE-PROTECT options at RESET.

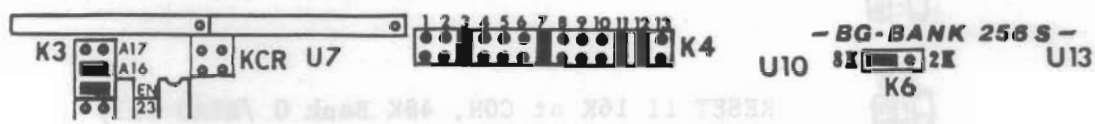
Hex output	Memory protected
RESET I	-NONE-

RESET II	-ALL-

02	8000-FFFF (top 32K)
01	-ALL-
00	-NONE-

No other outputs should go to the I/O port. In fact some 7-bit codes enable unpopulated memory locations.

D. LINEAR-128K of 8Kx8 RAM (partial population)



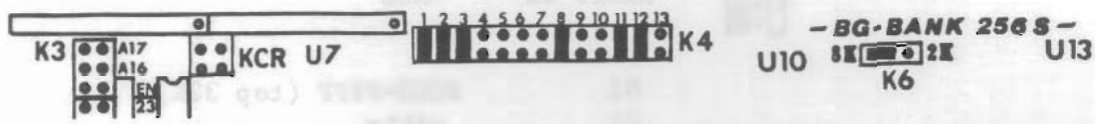
The memory is addressed as 128K of continuous memory. The memory may be in ay 128K window defined by jumpers A17-A23 of the extended address jumper, K3. Be sure that there is a jumper at K3-postion 2 and no jumper at K3-position 11 so that the extended address selects 128K windows. The 16 memory chips must be installed in the sockets corresponding to the lowest 128K block of the 256K memory. These locations are A1-A4, A6-A9, A10-A13, B1-B3, and C1.

BANK SELECT CONTROLS: The memory is not banked in the linear configuration. I/O controls may be output to WRITE-PROTECT the memory. The table assumes that the 128K of memory is located at the bottom of memory. The jumper setting at K7 also provides two WRITE-PROTECT options at RESET.

Hex output	Memory protected
RESET	-NONE-
RESET	-ALL-
08	18000-1FFFF (top 32K)
04	10000-1FFFF (top 64K)
02	08000-1FFFF (top 96K)
01	-ALL-
00	-NONE-

Any other output through the I/O port removes all WRITE-PROTECT.

E. MPM-System Bank plus 4 users:



The memory is arranged as one 16K bank at C000H always enabled and five 48K banks enabled by single bits through the I/O port.

Hex out	Memory enabled
RESET I	16K at C0H, 48K Bank 0 (system bank)
RESET II	16K at C0H, 48K Bank 0 /READ only
01	16K at C0H, 48K Bank 0 (system bank)
FE	BANK 0 READ-ONLY
02	16K at C0H, 48K Bank 1 (User 1)
FC	BANK 1 READ-ONLY
04	16K at C0H, 48K Bank 2 (User 2)
FB	BANK 2 READ-ONLY
08	16K at C0H, 48K Bank 3 (User 3)
F7	BANK 3 READ-ONLY
10	16K at C0H, 48K Bank 4 (User 4)
EF	BANK 4 READ-ONLY
20	16K at C0H
FD	16K at C0H
40	16K at C0H
FB	16K at C0H
80	16K at C0H
F7	16K at C0H

All other outputs enable 48K Bank 0 (system bank). Note that the five banks are normally enabled with single bit outputs. The complement of these outputs enables the banks for READ-ONLY. This is not normally used for MPM but this type of banking arrangement is ideal for PERMANENT RAM DISK implementations. (See the section on using the 256S as PERMAENT RAM).

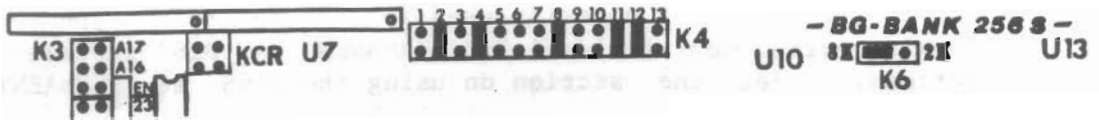
F. OASIS-System Bank plus 4 users:

The memory is arranged as one 16K bank at 00H always enabled and five 48K banks enabled by single bits through the I/O port.

	Hex out	Memory enabled
	RESET I	16K at 00H, 48K Bank 0 at 40H (system)
	RESET II	16K at 00H, 48K Bank 0 at 40H/READ only
	01	16K at 00H, 48K Bank 0 (system)
	FE	BANK 0 READ-ONLY
	02	16K at 00H, 48K Bank 1 (User 1)
	FC	BANK 1 READ-ONLY
	04	16K at 00H, 48K Bank 2 (User 2)
	FB	BANK 2 READ-ONLY
	08	16K at 00H, 48K Bank 3 (User 3)
	F7	BANK 3 READ-ONLY
	10	16K at 00H, 48K Bank 4 (User 4)
	EF	BANK 4 READ-ONLY
	20	16K at 00H
	FD	16K at 00H
	40	16K at 00H
	FB	16K at 00H
	80	16K at 00H
	F7	16K at 00H

All other outputs enable 48K Bank 0. The complements of the normal bank select words select a bank for READ-ONLY which means it is WRITE-PROTECTED. This protection is not normally used in the multi-user OASIS environment. However, this same banking arrangement can be used for PERMANENT RAM applications where the banks of RAM are to be treated as permanent code storage media. (See section on using the 256S as PERMANENT RAM).

G. AMOS I (Alpha Micro)-System plus 7 users



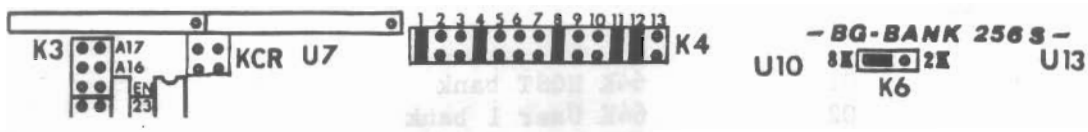
The memory is arranged as one 32K bank at 00H and sever 32K banks at 80H. The 32K bank at 00H is the system bank and the other seven banks are bankswitched in as user banks. This arrangement is for up to seven users on one 256S memory board. A second set of eight users may be accommodated on a second board using AMOS II described below.

	Hex out	Memory enabled
	RESET I	32K at 00H (system bank)
	RESET II	32K at 00H (system bank) and 32K at 80H (User 1 bank)
	01	32K User 1 bank at 80H
	FE	32K User I bank/READ only
	02	32K User 2 bank at 80H
	FD	32K User 2 bank/READ only
	04	32K User 3 bank at 80H
	FB	32K User 3 bank/READ only
	08	32K User 4 bank at 80H
	F7	32K User 4 bank/READ only
	10	32K User 5 bank at 80H
	EF	32K User 5 bank/READ only
	20	32K User 6 bank at 80H
	DF	32K User 6 bank/READ only
	40	32K User 7 bank at 80H
	BF	32K User 7 bank/READ only
	80	-NO USER BANK ENABLED-

For all of the above bank controls the system bank (32K at 00H) remains enabled. Any other outputs through the I/O port enable the system bank only.

The READ only output controls are not used in the standard AMOS system. They are included to allow WRITE protection for special RAM disk applications where this multiple 32K banking scheme is convenient.

H. AMOS II-Eight 32K USER banks



The memory is arranged simply as eight 32K banks of memory all addressed at 80H to be eight AMOS user banks.

Hex output	Memory enabled
RESET I	-NONE-

RESET II	32K at 80H/User 8 bank
01	32K at 80H/User 1 bank
FE	User 1 bank WRITE protected
02	32K at 80H/User 2 bank
FD	User 2 bank WRITE protected
..	.....
-similar continuation-	
..	.....
80	32K at 80H/User 8 bank
7F	32K at 80H but NOT write protected

I. CROMIX I - HOST plus 3 USERS

The memory is arranged as four 64K banks. On RESET only the lower 32K of the HOST bank is enabled. The four 64K blocks are the HOSt bank plus User 1,2, and 3. This arrangement is for 3-USER Cromix only. 4,5, or 6 User Cromix can be arranged using Cromix II described below.

A second RESET option exists only for special applications in which Cromix is to be used but the hardware booting arrangement is arranged differently.

Hex out	Memory enabled
RESET I	32K at 00H (top 32K OFF)

RESET II	64K at 00H
01	64K HOST bank
02	64K User 1 bank
04	64K User 2 bank
08	64K User 3 bank
10	64K HOST bank again
20	64K HOST bank
40	64K HOST bank
80	32K bottom half of HOST bank, top 32K of all banks

Any other outputs are equivalent to the RESET I option enabling 32K at 00H with all other memory disabled.

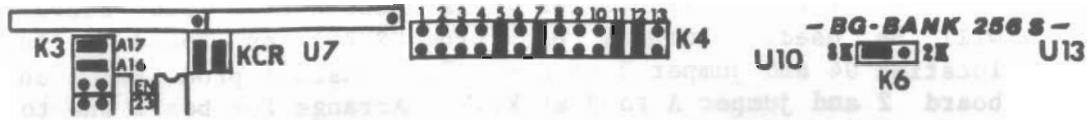
J. CROMIX II - Users 1,2,3,and 4

The memory is arranged as four 64K banks enabled as Users 1,2,3, and 4. The board is OFF on RESET. The board may be used with one, two, or three other 64K Cromemco compatible boards to make a 4-User, 5-User, or full 6-User CROMIX system. When using other boards with the 256S, they must be arranged as the HOST bank and Users 5 and 6 since the 256S is specifically arranged to be Users 1,2,3, and 4. If a full 6-User Cromix system is to be arranged using BG-BANK 256S boards, the special CROMIX-D PROM set must be used as described in the next section. (below)

Hex output	Memory enabled
RESET	-NONE-
01	-NONE-
02	64K - User 1 bank
04	64K - User 2 bank
08	64K - User 3 bank
10	64K - User 4 bank
20	-NONE-
40	-NONE-
80	Top 32K of Users 1,2,3, and 4

Any other output through the I/O port is an invalid Cromemco bank select and is equivalent to RESET (no memory enabled).

K. CROMIX-D: For use with Cromemco Z80/68000 DPU board



The Cromix D configuration is specifically for use with the Cromemco Dual-Processor board. While the Z80 processor is accessing the S-100 bus the memory is treated as standard Cromix multiuser memory accessed as bank selected 64K blocks. When the 68000 processor controls the bus, the same memory is to be 16-bit linear memory. Various arrangements are possible using one, two, or more 256S memory boards. The configurations described below all use the CROMIX-D SELECT PROM (U3 = CRDSEL) and the CROMIX-D BANK PROMS (U4 = CRDB01 or CRDB02).

For operation with the DPU processor card, two vertical jumpers must be installed at jumper area KCR. Also 16-bit data transfers must be enabled at K3-12. Finally extended addressing should not be enabled at K3-3 but jumpers should be at K3-1,2 and the 256K extended address window for the linear memory should be defined by the jumpers at K3: 4-9 (leave K3:10,11 open).

1. Host plus Users 1,2, and 3 - Single 256S board

For this configuration, it is assumed that only one 256S board is to be used. Replace U4 with the Cromix Bank Prom CRDB01 and jumper A to B at K7 (Reset I).

Hex output	Memory enabled
RESET	
	32K at 00H only
01	64K HOST bank
02	64K User 1 bank
04	64K User 2 bank
08	64K User 3 bank
10	64K HOST bank
20	64K HOST bank
40	64K HOST bank
80	32K bottom half of HOST bank Top 32K of all banks

Whenever the 68000 processor takes over the bus, the memory becomes a linear 256K block of memory enabled in a 256K window determined by the jumper settings at the extended address jumper area K3. Normally a single 256S board will be at the bottom of memory.

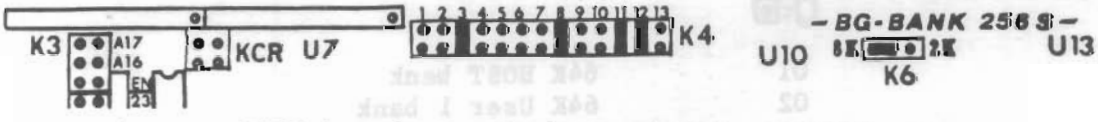
2. Host plus 6 Users - Two board system

For this configuration it is assumed that two boards will be used. Install bank prom CRDB01 on board 1 in location U4 and jumper B to C at K7. Install prom CRDB02 on board 2 and jumper A to B at K7. Arrange for board one to be the bottom 256K block of extended memory and for board two to be the second 256K block of extended memory. The bank selection will be as follows:

Hex output	Board 1	Board 2
RESET		
	32K of HOST	OFF
01	64K HOST bank	OFF
02	64K User 1 bank	OFF
04	64K User 2 bank	OFF
08	64K User 3 bank	OFF
10	OFF	64K User 4 bank
20	OFF	64K User 5 bank
40	OFF	64K User 6 bank
80	32K bottom of HOST Top 32K,Users 1-3	Top 32K of Users 4, 5, and 6

When the Z80 processor is controlling the bus, the 512K of memory supports a full 6-User Cromix system. When the 68000 processor takes over, the memory becomes 512K of linear memory. If system control is later returned to the Z80 processor, the memory enabled will be the same as the last bank that was enabled prior to the switch in control from the Z80 to the 68000 unless 68000 software has output a bank select to port 40H.

3. Full 6-User Cromix system using two boards but not using the Cromemco DPU board.

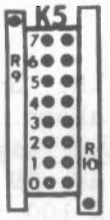


If two 256S boards are to be used for a full 6-User Cromix system but the conventional Z80 processor card is used instead of the Dual Processor card, the following procedure is required:

1. Arrange proms as above in section K.2
2. Do not place jumpers at KCR.

The 512K of memory will be arranged exactly as in section K.2 above except the memory will not become linear without jumpers at KCR. Memory access is controlled solely by bank selection and not by extended addressing.

K5:I/O PORT



The I/O port can be set to be any of 256 possible device codes. The device code is arranged with shorting jumpers at K5. A jumper corresponds to an address bit of 1 and no jumper corresponds to a zero. Eight data bits may be sent through the I/O port for bank selection and control. The control words are determined by a bank select PROM. The appropriate bank control words and their control functions are given with each memory configuration.

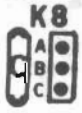
K6: RAM TYPE SELECTION

Jumper K6 is used to allow either 2Kx8 or 8Kx8 rams to be used. The 2Kx8 are 24 pin chips whereas the 8Kx8 are 28 pin chips. For 2Kx8 chips a jumper is placed between the center pin and the right pin at K6. Similarly, a jumper on the left side accommodates 8Kx8 chips. This jumper allows memory pin 23 to be the write-enable for 2Kx8 chips and A12 for 8Kx8 chips. Note that for 2Kx8 EPROMS (such as 2716), pin 23 of the 28 pin socket corresponds to the program pin. Consequently, 2Kx8 EPROMS may be mixed with 8Kx8 rams without difficulty. The user must note that such an arrangement leaves duplicate code in the 8K block filled with 2K code. In fact the 8K memory block will appear as four duplications of the 2K of EPROM code.

K7: I/O PORT ENABLE/DISABLE

If the I/O port on the board is to be used for any type of bank selection control or write protection, the port must be enabled at K7 by installing a jumper across E-P. When the I/O port is used, care must be taken to avoid any conflict of the 256S on-board port with any other device port used in the system. If no I/O controls are to be used with the 256S memory board, the port may be disabled by installing a jumper across P-D at K7. This avoids the need to worry about any I/O conflicts when the board is to be used as linear memory.

K8: BANK CONTROL OPTIONS



K8 allows two possible bank control options. Pin B is one input to the BANK PROM, IC-4, and may be connected to A or C. The standard jumper arrangement at K8 is AB but the possible options (i.e. BC jumpered) are defined in the MEMORY CONFIGURATIONS section.

K9: POWER-FAIL SENSE SIGNAL (Battery backup users only)

The Power-Fail sense circuitry monitors the unregulated +8 volt supply line of the S-100 bus. When this voltage drops to about 7.5 volts, the sense circuitry generates a low-going signal driven by an open collector that may be jumpered at K9 to pull the Non-Maskable-Interrupt line of the bus (S-100 pin 12) or the Power-Fail-Sense line (S-100 pin 13). The signal indicates that a power drop is occurring. The processor can service the interrupt in a number of ways. It may save all registers and go into a HALT or into a loop. It may save the registers, turn off the memory board and then fetch FFs. Normally at power failure time, the processor will have 10 to 30 milliseconds before the unregulated voltage has dropped another 0.5 volts to 7.0 volts. At this level, the Power-Fail-Sense circuitry disables the board so that it is totally isolated for reads or writes. Note that the sense circuitry has significant hysteresis so that these sense signals will not rapidly recur. However, when the bus power returns to +8 volts, the board isolation is no longer enabled and the board may function normally. An alternate procedure for accomodating power failure is to have the signal which normally would isolate the memory board also pull the RESET line of the processor. Then when normal power is restored, the processor starts up as if from RESET. In such an arrangement the system booting program would write a message in the battery supported RAM saying "system up". When the system starts from RESET, part of the initialization program would be to check to see whether this should be a "cold" start or a "warm" start. The processor could return to normal processing after "warm" starts which would accompany power failures. A simple modification is described in the reference section for pulling the RESET line with an open-collector circuit.

K10: PHANTOM AND DIRECT-MEMORY-ACCESS ENABLE

Jumpers at K10 can be connected to enable PHANTOM to the board or to disable the board for DMA transfers. For the standard memory configurations, when PHANTOM is enabled, it is enabled for the entire board. Likewise when DMA is jumpered, the entire board is disabled for DMA transfers. However, PHANTOM and DMA are inputs to a STATUS PROM. The memory configuration PROM can be custom programmed to selectively enable PHA and/or DMA for chosen banks of memory or memory address windows.

III. SPECIAL APPLICATIONS REFERENCE SECTION

The following section details the applications that make use of the many available features of the BG-BANK 256S CMOS memory board.

A. RAM-EPROM MIXING

The standard RAM chip used with the 256S is a 28-pin 8Kx8 chip. However, the board will also accommodate 24-pin 2Kx8 memory chips. RAM and EPROM may be easily mixed if they are the same memory size. For example, 28-pin 8Kx8 RAM and 28-pin 2764 EPROMs (also 8Kx8 memories) may be used interchangeably. These both require that the jumper at K6 be set for 8K memory. The 2732 EPROM is a 24-pin chip but is compatible with the 8Kx8 pin configuration. However it is a 4Kx8 PROM addressed by 12 addresses. Consequently, the 13th address which is connected at pin 2 of the 28-pin socket will be ignored. The 4K of code in the 2732 will appear in both the upper and lower 4K of the 8K memory space. Similarly, 2716 EPROMs (2Kx8) may be used in the 28-pin sockets mixed with 8Kx8 RAM but both the 12th and 13th addresses at the 28-pin memory socket will be ignored and the 2K of code in the 2716 will appear 4 times in the 8K memory space. The important thing to note is that 8Kx8 RAM may be mixed with 2764 (8Kx8), 2732(4Kx8), or 2716 (2Kx8) single voltage EPROMS.

B. EPROM PROGRAMMING

The 256S board is designed to accommodate both 8 and 16 bit data transfers. For 16 bit transfers, A0 is ignored and two memory chips are enabled simultaneously to provide a 16 bit word. The net result is that EPROM must be programmed in the standard manner for 16-bit data. For 8-bit code this means that in a given 16K memory block, one chip will contain 8K of EVEN-ADDRESS code and a complimentary chip will contain the matching 8K of ODD-ADDRESS code. The memory address translation is effectively to disregard A0, divide the memory address by 2, and program the resulting location in the EVEN or ODD EPROM depending on A0.

The result is that EPROMS must be programmed in pairs containing the EVEN and ODD addressed code. The following simple 8080 program will assemble 16K (8K,4K) of code into an 8K EVEN block (4K, 2K) and an 8K ODD block (4K, 2K) for programming a pair of 2764 (2732, 2716) EPROMS.

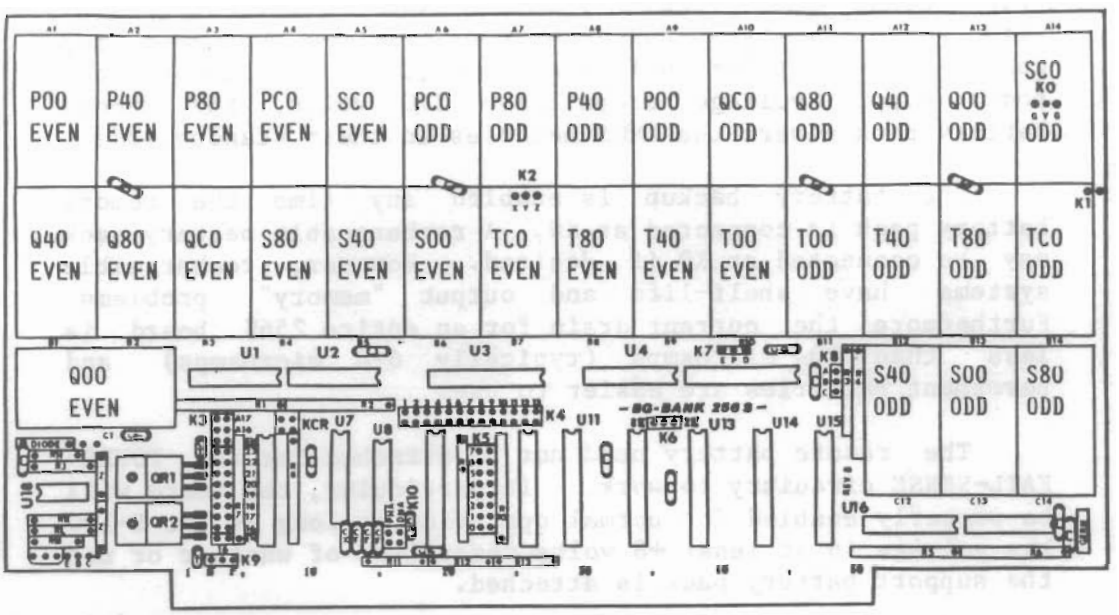
```
TRANSLATE:    LXI H,PROM      ;PROM=EPROM CODE LOCATION
              LXI D,CODE      ;CODE=SOURCE FOR EPROMS
              LXI B,SIZE      ;SIZE=EPROM WORD CAPACITY
EVEN:         LDAX D          ;1ST CODE BYTE INTO ACCUM.
              MOV M,A         ;LOAD TO (HL)
              INX H           ;INCREMENT HL
              INX D           ;INCREMENT DE
              INX D           ;    BY TWO
              DCX B           ;DECREMENT BYTE COUNTER
              MOV A,B         ;CHECK B FOR LESS THAN ZERO
              CPI FF          ;BC=FFFF?
              JZ ODD          ;ASSEMBLE SECOND BLOCK
              JP EVEN         ;FINISH "SIZE" BYTES
ODD:          LXI B,SIZE      ;SIZE=EPROM WORD CAPACITY
              LXI D,CODE      ;SOURCE CODE LOCATION
              INX D           ;DE=1ST ODD BYTE
ODD1:         LDAX D          ;LOAD BYTE FROM DE
              MOV M,A         ;  TO HL LOCATION
              INX D           ;POINT TO NEXT
              INX D           ;  ODD BYTE
              INX H           ;POINT TO NEXT MEMORY LOC
              DCX B           ;DECREASE BYTE COUNTER
              MOV A,B         ;CHECK B FOR LESS THAN ZERO
              CPI FF          ;BC=FFFF?
              JZ STOP         ;IF DONE, STOP
              JP ODD1         ;LOOP FOR "SIZE" BYTES

STOP:         RET (OR CONTINUE, ETC.)
```

As an example, one could be trying to assemble 8K of code to program into two 2732 EPROMS. Suppose the correct code is located at 100H and the EPROM source location is to be 4000H. Then in the above program, PROM = 1000H, CODE = 100H, SIZE = 1000H or 4096 8-bit words. The 8K of source code would be in memory from 100H to 2100H. The program would move all the even bytes to 4000H-4FFFH and all the odd bytes to 5000H-5FFFH. The EVEN 2732 could be programmed from code at 4000H-4FFFH and the ODD 2732 programmed from code at 5000H-5FFFH.

C. EPROM POSITIONING:

The 256S memory board may be pictured as being made up of four 64K blocks of memory consisting of 8 memory chips each. These blocks will be labelled P, Q, S, and T. For the linear 256K configuration, block P is addressed at 00000H, Q at 10000H, S at 20000H, and T at 30000H (if the 256K is the bottom 256K window of memory). Pairs of memory chips (8Kx8) are addressed on 16K boundaries with one enabled by even addresses and the complementary pair enabled by odd addresses. The figure below shows the memory locations.



Block T is at the top of the 256K window in the linear mode. The table below clarifies address locations

T00-EVEN (ODD)	30000-33FFF, EVEN (ODD)
T40-EVEN (ODD)	34000-37FFF, EVEN (ODD)
T80-EVEN (ODD)	38000-3BFFF, EVEN (ODD)
TC0-EVEN (ODD)	3C000-3FFFF, EVEN (ODD)

EPROMS may be located anywhere. However, block T is the memory block whose power bus may be isolated from the memory array power bus and connected to the TTL logic supply. This isolation is described in the configuration guide, jumper area K1-K2. With this power division possibility, a board may be arranged to have a mixture of EPROM and battery-backed CMOS RAM.

D. USING THE 256S WITH BATTERY BACKUP:

The battery backup option allows continuous retention of memory contents during power failures or during intentional

power shutdowns. The POWER-FAIL-SENSE circuit monitors the unregulated +8 volt supply line from the S-100 bus. Any time this voltage drops below about 7.8 volts, the circuit provides an open-collector driven negative signal that may be jumpered to NON-MASKABLE-INTERRUPT (pin 12) or POWER-FAIL (pin 13) of the bus. This signal selection is made at jumper area K9. When the voltage decays another 0.5 volts, the board access is eliminated isolating the board from spurious writes to memory. For the typical power failure the processor has 10 to 20 milliseconds between the POWER-FAIL signal and the BOARD-DISABLE signal. This provides more than adequate time for the processor to jump to a service routine which stores all CPU register information for later restart. With an appropriate POWER-ON program, the processor may continue where it left off after POWER-UP. Any time the on-board supply voltage drops below 3.0 volts, the remote battery pack powers the CMOS memories in their standby mode.

The battery backup is enabled any time the remote battery pack is connected at K0. A rechargeable battery pack may be connected at K0 if desired. However, rechargeable systems have shelf-life and output "memory" problems. Furthermore the current drain for an entire 256K board is less than 20 microamps (typically 6-8 microamps) and permanent batteries are easier to use.

The remote battery need not be attached for the POWER-FAIL-SENSE circuitry to work. In particular, the board will be properly enabled for normal operation as long as the S-100 bus voltage is at least +8 volts regardless of whether or not the support battery pack is attached.

E. POWER-DOWN-PRECAUTIONS:

The BG-BANK 256S may be used as permanent alterable memory allowing the storage of mixtures of firmware and data without the need for disk file generation. Two 256S boards represents a half-megabyte ultra-fast disk. The board can be write protected and the memory left in the retention mode after normal power-down. However, care must be taken to avoid spurious CPU fetches at power down. When the normal computer system is powered up, the CPU is held initially RESET by the POWER-ON-CLEAR signal to the processor. This avoids possible spurious CPU processing during power voltage stabilization. No such POWER-DOWN signal is generated. Consequently, the CPU typically fetches erroneous code or receives spurious bus signals such as interrupts long before the power even begins to drop. The spurious CPU operation is caused by switch noise. The 256S contains power-fail-sense circuitry and is protected against power failure but spurious CPU processing at POWER-DOWN must be avoided. There are various procedures which avoid this problem. They are listed below for simplicity.

1. Hold the system RESET button down while switching off the system.

2. Use WRITE-PROTECT I/O instructions to protect the memory prior to shutdown (see memory configurations). These instructions are sent through the I/O port on the 256S which may be any of 256 device codes.

If POWER-DOWN precautions are taken, the memory may be treated as alterable PROM indefinitely.

F. USING THE BG BANK 256S AS PERMANENT RAM:

The 256S is particularly suitable for use as a memory disk or as software-alterable PROM. Two of the possible memory configurations for multi-users are particularly suitable for RAM-DISK. The MPM arrangement consists of a 16K block of memory addressed at C0H which is always enabled and five 48K banks of memory located at 00H and switched in through bank select. The same arrangement could be used for a single user under CP/M using 64K with four 48K banks or 192K of memory which is accessed as disk by bank selection. The Alpha Micro memory configuration allows the 256K of memory to be eight 32K banks enabled by bank select and addressed at 80H. For a single user, 64K would be available as system memory and the remaining 192K would be six 32K banks located at 80H accessed as disk via bank selection.

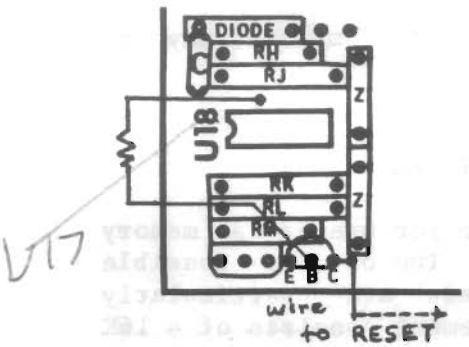
In these memory configurations, the software write-protect is sent out as the complement of the I/O data that enables a given bank. Therefore a bank may be enabled for READ-WRITE with a hex output of, say, 04 or enabled for READ-ONLY with a hex output that is the complement of 04 or FB.

G. BATTERY BACKUP WITH MULTIPLE BOARDS:

Each board comes with a tag on the back side at the battery connector indicating two measured voltages. These refer to levels of the unregulated supply voltage to the board. The higher voltage is the level at which a POWER-FAIL-SENSE signal is generated. The lower level is the level at which ACCESS to the memory is disabled. When using multiple BG BANK boards (256S or 64S), only one board should have the sensing signal connected to the S-100 bus. The board with the highest value of the ACCESS disable voltage should be the one jumpered to send the signal to the S-100 bus. This will insure that other boards are not disabled before the processor has had adequate time to operate a POWER-FAIL interrupt routine.

H. RESET CPU at Power-Fail (modification):

This modification is for use with battery-backed systems when it is desired to have the Power-Fail-Sense circuit hold the processor reset at the same time the board becomes isolated. The modification is done in the lower left hand corner of the board.



Modification:

1. Solder a NPN switching transistor (i.e. 2N3904) into the three holes immediately to the right of the existing transistor with leads emitter-base-collector from left to right. The added transistor will look the opposite of the existing transistor.
2. Solder a 10K 1/4 or 1/8 watt resistor on the bottom side of the board from U17-7 to the base lead of the transistor.
3. Solder a wire from the hole right at the top edge of the edge tab connector pin 75 (CPU reset) to the collector using the remaining hole adjacent to the collector lead of the installed transistor.

This modification will pull the Reset line low with an open-collector circuit when the unregulated voltage to the board drops below the level for board READ/WRITE isolation.

IV. WARRANTY INFORMATION:

The BG-BANK 256S is warranted for a period of one year from the date of purchase against defects in materials or workmanship. Should this product fail to perform satisfactorily, arrangements should be made with BG COMPUTER APPLICATIONS for warranty service as follows:

Return of the board is subject to the issuance of a RETURN MERCHANDISE AUTHORIZATION number by BG COMPUTER APPLICATIONS. The RMA number must be clearly visible on the outside of the returned package which is to be returned postage prepaid. Only packages with registered RMA numbers will be accepted.

BG COMPUTER APPLICATIONS will, at our option, repair or replace defective units received during the warranty period. This warranty is invalid if the product has been misused or modified. Warranty is limited to replacement of defective parts and no responsibility is assumed for damage to other equipment.

This warranty is made in lieu of all other warranties expressed or implied.

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Mr. John Monahan
Vitasoft Associates
Box 3037
Clifton, N.J. 07012

Dear John,

Again I wish to thank you for your patience and help during the last few weeks. I think the 256S problems are now solved. Solutions are always trivial in retrospect but the A0 polarity error was a very elusive rascal to find. Any memory test does writes followed by reads of either bytes or words but not mixed. I finally found the problem by writing a program that did word block moves and examining the results. The little monitor that did the examining did all byte reads. The bytes came out reversed and in an instant I knew the problem. I have reprogrammed the status prom to correct this problem.

I have included parts to first of all check board 6 and subsequently modify boards 1 through 5. You will find attached a suggested test procedure and a field update note.

I hope the boards will work for you now. They have been tested with the Lomas board at 10 Mhz and the Seattle Products board at 8 Mhz.

Thanks again for the help.

Yours truly,

Philip J. Green

Philip J. Green

VITASOFT ASSOCIATES

SUGGESTED TEST PROCEDURE

You have five 256S boards with no modifications and a sixth with mods. Included in the hardware is a status prom labelled STAT-6. This prom is to be a replacement on board 6 which can be distinguished by the pullups attached to its back side. With this new prom, board 6 should run properly. This prom is slightly different from the other five new proms labelled ST-0A. The modification that improves the noise immunity is to require DBIN to be true to turn on the Data-In buffers. This delays the time when the data bus is driven until after the addresses are latched. On board 6 this was included through pin 19 of the status prom at the expense of the WRITE-PROTECT feature of the board. The new modification includes this DBIN-true requirement through pin 3 of the Status prom and preserves all the other features of the board. Therefore the modification procedure has been changed since you received board 6. For your application as straight high-density memory, all the boards will essentially be the same. I have included a sixth ST-0A prom in case you choose to keep all the boards and wish to modify board 6 to match the other 5.

SUGGESTED TEST PROCEDURE:

Step 1: Replace Status prom in board 6 with STAT-6 and test.

Step 2: Replace U10 and U11 with the red high-profile modules labelled U10 and U11 in board 6 and test. (Hopefully this step will not be necessary but I would like to know the result, if possible.)

Step 3: If board 6 performs properly, modify one of the previous five boards as per the attached field-update note and test.

P.S. I would like to get the little red modules returned if possible. They include a 74LS244 arranged as a pin-replacement for the 74LS373 and they are quite hard to make. Thanks.

FIELD UPDATE

BG-BANK 256S MEMORY BOARD

I. Purpose: To arrange for the 256S memory module to correctly handle mixed 8 and 16-bit data transfers.

Procedure:

1. Cut the trace coming up from near the S-100 bus to pin 3 of U8, the STATUS prom. (see attached figure)

2. Solder a wire from U7-pin 9 to U8-pin 3.

3. Replace U8 (TBPSA42N) with the new status prom, ST-0A.

II. Purpose: To increase the noise immunity of the 256S.

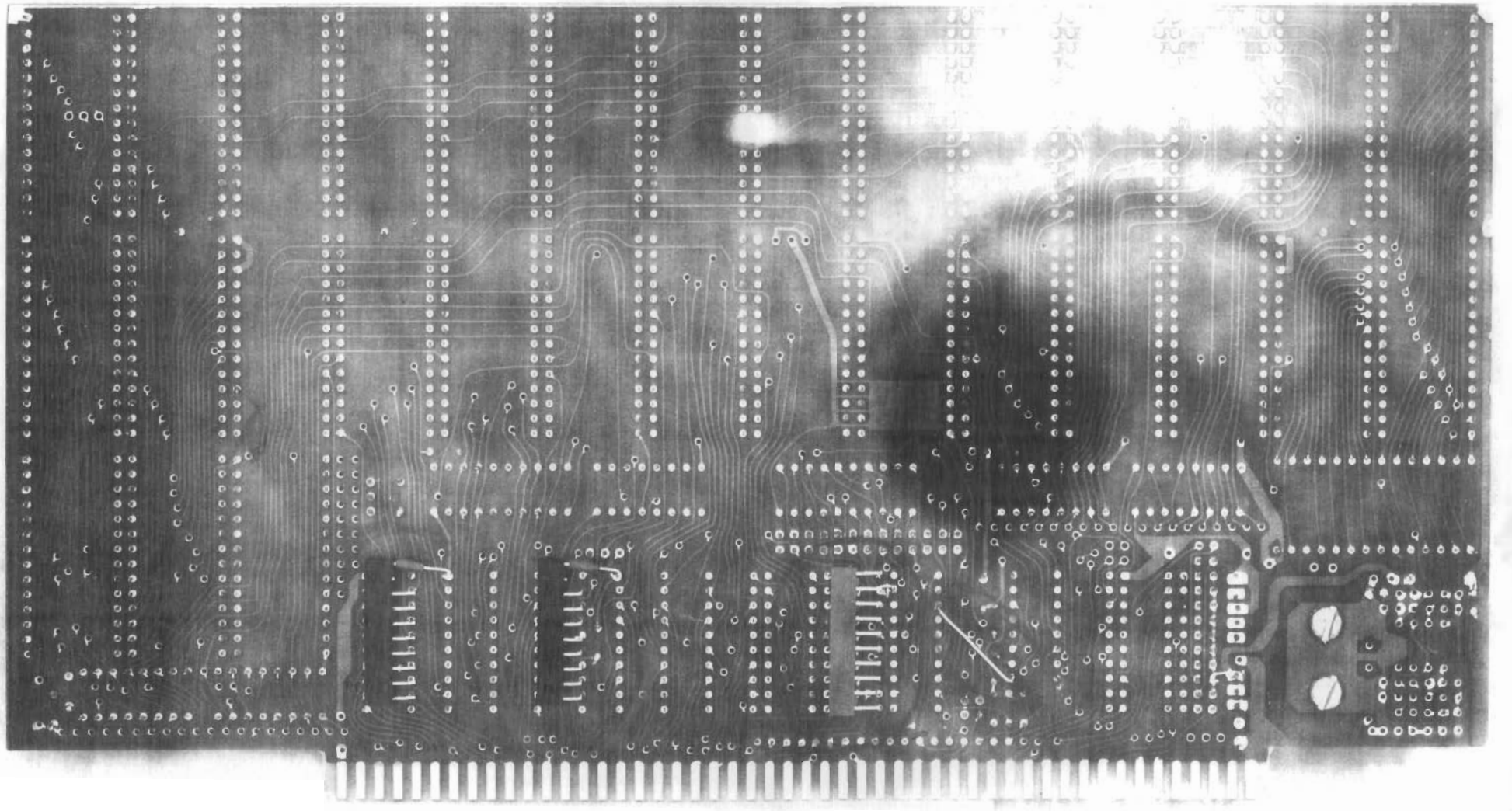
Procedure:

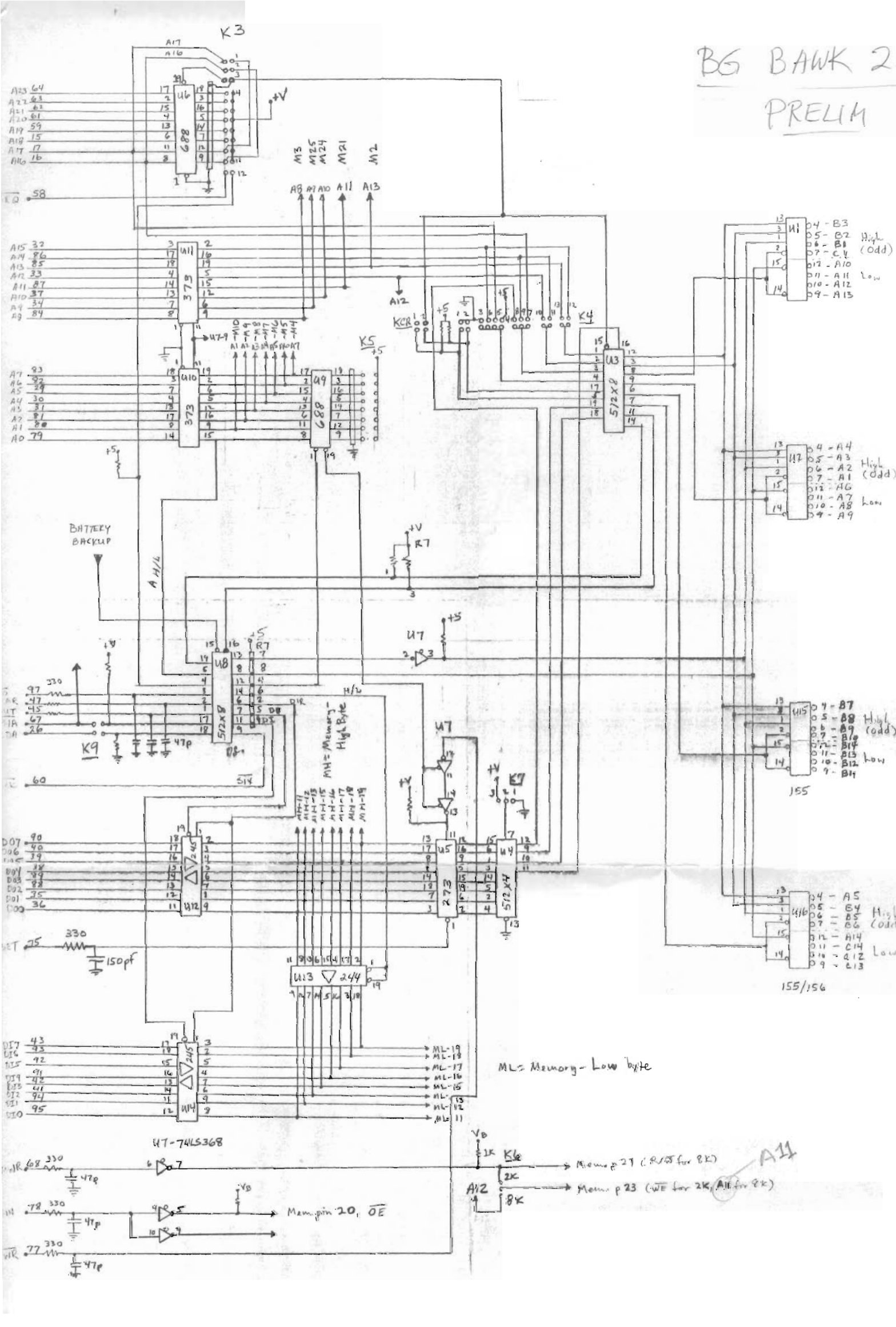
1. Solder pullup resistors to pins 2-9 of U12 and U14 using special 1K pullup packages with pin 2 removed. (see attached figure)

2. Solder a 1K 10-pin pullup package directly across the 10-pin SIP immediately to the right of U8. The common pin of the attached SIP should be up. This simply makes the net pullup resistance 500 ohms for faster recovery of the open collector outputs of the status prom. This procedure is not required unless the board is to operate at clock speeds of 8 Mhz or higher.

These modifications preserve all the features described in the 256S manual and provide an 256K memory that may be used with 8 and 16 bit processors at clock speeds of 8 to 10 Mhz. The board with these modifications has shown proven performance with fast 16-bit processor boards such as the Lomas Lightning One and the Seattle Computer Products 8086-87 board. With the large number of possible memory configurations, the board is also ideal for updating of Z80 systems to the 8 Mhz Z80H.

- 1K pullups on U12, U14 pins 2-9. Common SIP pin connected to +V of adjacent IC.
- 1K pullups on Status Prom
- Wire connecting U7-p9 to U8-p3
- Trace cut isolating U8-p3.




BG BAWK 2
PRELIM
K3
A17
A16
U6
688
+V
M3 M25 M24 M21 M2
A8 A9 A10 A11 A13
A12
U11
373
U10
373
U9
688
KCR
K4
K5
U3
512x8
U1
U2
U15
U16
High (Odd)
Low
BATTERY BACKUP
R7
U8
512x8
K9
47p
330
150pf
MH = Memory - High Byte
U7
U5
273
U4
512x4
K7
U12
245
U13
244
U14
245
ML = Memory - Low byte
74LS368
K6
1K
2K
8K
A11
A12
Mem pin 27 (R/W for 8K)
Mem pin 23 (WE for 2K, A11 for 8K)
Mem pin 20, OE
155
155/156